Apacer

Industrial microSD Card 6.1

CH120-MSD Product Specifications

January 14, 2025

Version 1.2

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Product Features

- Compliant with SD Memory Card Specifications
  - Part 1 Physical Layer Specification Ver6.1
  - Part 2 File System Specification Ver3.0
  - Part 3 Security Specification Ver4.0
- Capacity: 16, 32, 64, 128 GB
- NAND flash type: Kioxia TLC BiCS5 112 layers
- Firmware version: SLC-liteX
- Operating voltage range: 2.7V~3.6V
- microSD card form factor: 15mm (L) x 11mm (W) x 1mm (H)
- Temperature range
  - Operating: -25°C to 85°C (Standard) / -40°C to 85°C (Wide)
  - Storage: -40°C to 85°C
- Speed class: Class 10, A2, U3, V30
- Supports SD and SPI modes
- Bus Speed Mode[1] (using 4 parallel data lines): UHS-I mode
  - SDR12: SDR up to 25MHz 1.8V signaling
  - SDR25: SDR up to 50MHz 1.8V signaling
  - SDR50: 1.8V signaling, frequency up to 100MHz, up to 50 MB/sec
  - SDR104: 1.8V signaling, frequency up to 208MHz, up to 104 MB/sec
  - DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50 MB/sec
- Flash management
  - Built-in advanced ECC algorithm, Global Wear Leveling, Flash Bad-Block Management, Power Failure Management, Flash Translation Layer: Page Mapping, S.M.A.R.T., SMART Read Refresh™
- Enhanced security
  - Built-in write protection features (permanent and temporary)
  - Copyrights Protection Mechanism (Compliant with the highest security of SDMI standard)
- High reliability
  - Specifically designed for the industrial market, ideal for read-intensive applications such as navigation, infotainment, POS/POI systems, medical devices, and general boot media use cases
  - Supports MTBF of more than 3,000,000 hours
  - Supports up to 30,000 P/E cycles
  - Supports up to 10,000 card insertions and removals
  - Supports Copy Protection for Recorded Media (CPRM) for music and other commercial media
- RoHS Compliant

Note 1: Timing in 1.8V signaling is different from that of 3.3V signaling.

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Table of Contents

1. General Description 4

2. Functional Block 4

3. Electrical Interface Outlines 5

3.1 microSD Card Pin Assignment 5

3.2 microSD Card Bus Topology 5

4. Product Specifications 6

4.1 Capacity 6

4.2 Performance 6

4.3 Mean Time Between Failures (MTBF) 6

4.4 Endurance 7

4.5 Reliability and Durability 7

4.6 Certification and Compliance 8

5. Flash Management 9

5.1 Error Correction/Detection 9

5.2 Global Wear Leveling 9

5.3 Bad Block Management 9

5.4 Power Failure Management 9

5.5 Flash Translation Layer – Page Mapping 9

5.6 SLC-liteX 10

5.7 S.M.A.R.T. 10

5.8 SMART Read Refresh™ 10

6. SD Card Comparison 11

7. Electrical Specifications 13

7.1 Absolute Maximum Rating 13

7.2 Power Requirement 13

7.3 Power Consumption 13

7.4 DC Characteristics 13

7.4.1 Bus Operation Conditions for 3.3V Signaling 13

7.4.2 Bus Signal Line Levels 14

7.5 AC Characteristics 15

7.5.1 microSD Interface Timing (Default) 15

7.5.2 microSD Interface Timing (High-Speed Mode) 16

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7.5.3 microSD Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes) 17
7.5.4 microSD Interface Timing (DDR50 Mode) 19

8. S.M.A.R.T. 21

8.1 Direct Host Access to SMART Data via SD General Command (CMD56) 21
8.2 Process for Retrieving SMART Data 22

9. Mechanical Dimensions 24

10. Product Ordering Information 27

10.1 Product Code Designations 27
10.2 Valid Combinations 27

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1. General Description

Apacer CH120-MSD microSD card is fully compatible with microSD card version 6.1, adhering to the [Physical Layer Specification Ver6.1 Final] definitions. It supports both the Non-secure Area and Secure Area capacities, following the [Part 3 Security Specification Ver4.0 Final] standards.

The microSD card features an 8-pin interface, allowing it to switch between SD mode and SPI mode communication protocols. It efficiently performs data error detection and correction with very low power consumption and supports capacities of up to 128GB with exFAT SDXC.

With its high performance, reliable functionality, and wide compatibility, Apacer CH120-MSD microSD card is a popular choice in semi-industrial and medical markets, offering customized firmware solutions to meet specific application needs.

2. Functional Block

The microSD contains a card controller and a memory core for the SD standard interface.

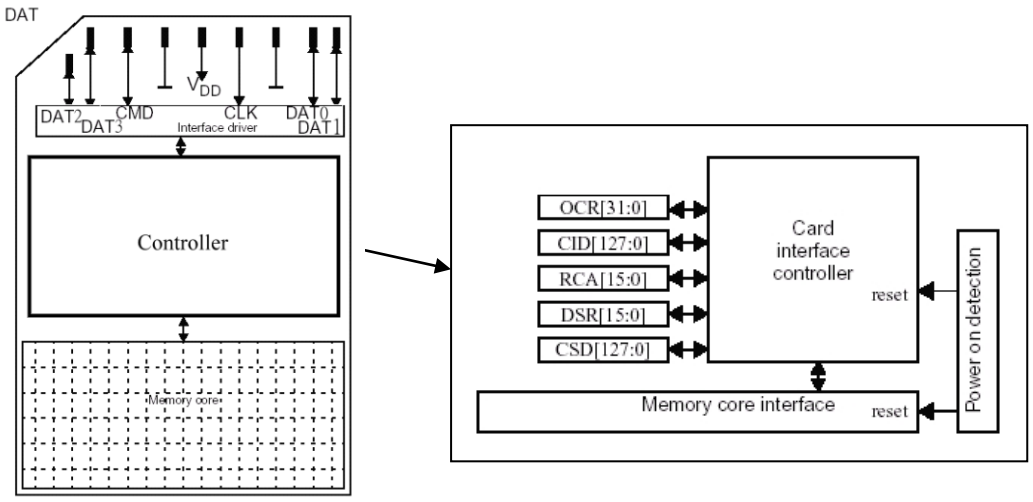


Figure 2-1 Functional Block Diagram

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3. Electrical Interface Outlines

3.1 microSD Card Pin Assignment

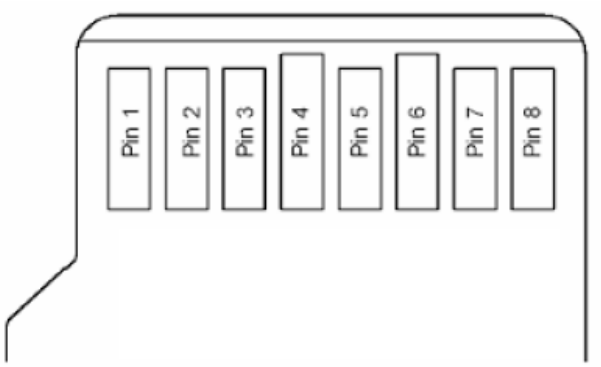


Figure 3-1 microSD Card Pin Assignment

Table 3-1 microSD Card Pin Assignment

Pin	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type	Description
1	DAT2	I/O/PP	Data Line [bit 2]	RSV		
2	CD/DAT3[2]	I/O/PP[3]	Card Detect/ Data Line [bit 3]	CS	I[3]	Chip Select (negative true)
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [bit 0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [bit 1]	RSV		

Notes:
1. S: power supply, I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers.
2. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3. At power up, this line has a 50KOhm pull up enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode, it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user during regular data transfer with SET_CLR_CARD_DETECT (ACMD42) command.

3.2 microSD Card Bus Topology

The microSD card supports two communication protocols: SD and SPI. The host system can choose either one of these modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same mode. The SD mode supports 4-bit high-performance data transfer, while the SPI mode offers only 1-bit data transfer, delivering lower performance than SD mode.

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4. Product Specifications

4.1 Capacity

The following table shows the specific capacity for CH120-MSD.

Table 4-1 Capacity Specifications

Capacity	Total bytes
16 GB	16,007,561,216
32 GB	32,107,397,120
64 GB	64,221,085,696
128 GB	127,859,163,136

Note: Total bytes are viewed under Windows operating system and measured by SD format.

4.2 Performance

Performance of CH120-MSD is shown in the table below.

Table 4-2 Performance Specifications

Capacity	Speed Class	Sequential (MB/s)		4K Random (IOPS)	
		Read	Write	Read	Write
16 GB	C10 U3 V30 A2	90	75	1,900	1,100
32 GB	C10 U3 V30 A2	90	80	1,900	1,100
64 GB	C10 U3 V30 A2	90	80	1,900	1,100
128 GB	C10 U3 V30 A2	90	80	1,900	1,100

Notes:
- Results may differ from various flash configurations or host system setting.
- Sequential read/write is based on CrystalDiskMark 8.0.4 with file size 1,000MB.
- Random read/write is measured using IOMeter with Queue Depth 32.
- Performance results are measured based on USB 3.0 card reader.

4.3 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) indicates a device's reliability by representing the average time between one repair and the next failure. This metric is usually expressed in hours. A higher MTBF value signifies greater device reliability.

Table 4-3 Mean Time Between Failures

Analysis Method	MTBF (Hours)
Telcordia Technologies Special Report, SR-332, Issue 3 method	>3,000,000

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4.4 Endurance

The endurance of a storage device is predicted by TeraBytes Written based on several factors related to usage, such as the amount of data written into the drive, block management conditions, and daily workload for the drive. Thus, key factors, such as Write Amplifications and the number of P/E cycles, can influence the lifespan of the drive.

Table 4-4 Endurance Specifications

Capacity	TeraBytes Written
16 GB	363
32 GB	568
64 GB	129
128 GB	334

Notes:
- Flash vendor guaranteed 3D SLC-liteX P/E cycles: 30K
- WAF may vary from capacity, flash configurations and writing behavior on each platform.
- 1 Terabyte = 1,024 GB

4.5 Reliability and Durability

Table 4-5 Reliability and Durability

Parameter		Specification
Temperature	Operating	-25°C to 85°C (Standard); -40°C to 85°C (Wide)
	Storage	-40°C to 85°C
Shock		1,500G, 0.5ms
Vibration		20Hz~80Hz/1.52mm (frequency/displacement) 80Hz~2000Hz/20G (frequency/displacement) X, Y, Z axis/60mins each
Drop		150cm free fall, 6 face of each
Bending		≧10N, hold 1min/5times
Torque		0.1N-m or 2.5deg, hold 5min/5times
Salt Spray		Concentration: 3% NaCl at 35°C (storage for 24 hours)
Waterproof		JIS IPX7 compliance. Water temperature: 25°C Water depth: the lowest point of unit is locating 1000mm below surface (storage for 30 mins)
X-Ray Exposure		0.1 Gy of medium-energy radiation (70 KeV to 140 KeV, cumulative dose per year) to both sides of the card (storage for 30 mins)
Durability		10,000 times mating cycle
ESD		Pass

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4.6 Certification and Compliance

Apacer CH120-MSD complies with the following standards:

- CE
- UKCA
- FCC
- BSMI
- RoHS
- EMI
- ESD

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5. Flash Management

5.1 Error Correction/Detection

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, the microSD card applies the BCH ECC Algorithm, which can detect and correct errors occurring during the read process, ensure data has been read correctly, as well as protect data from corruption.

5.2 Global Wear Leveling

NAND Flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some area get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Global Wear Leveling technique is applied to extend the lifespan of NAND Flash by evenly distributing writes and erase cycles across the media.

Apacer provides Global Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing Global Wear Leveling algorithm, the life expectancy of the NAND Flash is greatly improved.

5.3 Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Apacer implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

5.4 Power Failure Management

Apacer industrial SD and microSD cards provide complete data protection mechanism during every abnormal power shutdown situation, such as power failure at programming data, updating system tables, erasing blocks, etc. Apacer Power-Loss Protection mechanism includes:

- Maintaining data correctness and increasing the reliability of the data stored in the NAND Flash memory.
- Protecting firmware table and the data written to flash from data loss in the event of power off.

5.5 Flash Translation Layer – Page Mapping

Page mapping is an advanced flash management technology whose essence lies in the ability to gather data, distribute the data into flash pages automatically, and then schedule the data to be evenly written. Page-level mapping uses one page as the unit of mapping. The most important characteristic is that each logical page can be mapped to any physical page on the flash memory device. This mapping algorithm allows different sizes of data to be written to a block as if the data is written to a data pool and it does not need to take extra operations to process a write command. Thus, page mapping is adopted to increase random access speed and improve microSD lifespan, reduce block erase frequency, and achieve optimized performance and lifespan.

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5.6 SLC-liteX

SLC-liteX is based on 3D NAND technology. The firmware is carefully tweaked by our engineering team so as to offer the greatest number of P/E cycles in this format – 30,000, which is 10 times more than MLC or industrial 3D TLC. The longest lifespans are therefore available at reasonable cost.

5.7 S.M.A.R.T.

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is a special function that allows a memory device to automatically monitor its health. Apacer provides a program named SmartInfo Tool to observe Apacer's SD and microSD cards. Note that this tool can only support Apacer's industrial SD and microSD cards. This tool will display firmware version, endurance life ratio, good block ratio, and so forth.

5.8 SMART Read Refresh™

Apacer's SMART Read Refresh plays a proactive role in avoiding read disturb errors from occurring to ensure health status of all blocks of NAND flash. Developed for read-intensive applications in particular, SMART Read Refresh is employed to make sure that during read operations, when the read operation threshold is reached, the data is refreshed by re-writing it to a different block for subsequent use.

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6. SD Card Comparison

Table 6-1 Comparing SDSC, SDHC, and SDXC

Item	SDSC	SDHC	SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v – 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

Table 6-2 Comparing Speed Class Symbols

Item	C2 (Class 2)	C4 (Class 4)	C6 (Class 6)	C10 (Class 10)
Bus Mode	UHS-I/UHS-II			
SD Memory Card	SDSC, SDHC, SDXC			
Mark				
Min. Sequential Write Speed	2 MB/s	4 MB/s	6 MB/s	10 MB/s

Table 6-3 Comparing UHS Speed Grade Symbols

Item	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Bus Mode	UHS-I/UHS-II	
SD Memory Card	SDHC, SDXC	
Mark		
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording real-time broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

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Table 6-4 Comparing Video Speed Class Symbols

Item	V6 (Video Speed Class 6)	V10 (Video Speed Class 10)	V30 (Video Speed Class 30)	V60 (Video Speed Class 60)	V90 (Video Speed Class 90)
Bus Mode	High Speed/UHS-I/UHS-II		UHS-I/UHS-II	UHS-II	
SD Memory Card	SDHC, SDXC				
Mark					
Performance	6 MB/s minimum write speed	10 MB/s minimum write speed	30 MB/s minimum write speed	60 MB/s minimum write speed	90 MB/s minimum write speed
Applications	HD/FHD Video Recording	FHD Video Recording, HD Still Image, Continuous Shooting.		4K/2K Video Recording	8K/3D/360° Video Recording

Table 6-4 Comparing Application Performance Class Symbols

Item	A1 (Application Performance Class 1)	A2 (Application Performance Class 2)
Mark		
Min. Random Read	1500 IOPS	4000 IOPS
Min. Random Write	500 IOPS	2000 IOPS
Min. Sustained Sequential Write	10 MB/s	10 MB/s
Applications	Main target is uSD for Android mobile handset	

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7. Electrical Specifications

7.1 Absolute Maximum Rating

Table 7-1 Absolute Maximum Rating

Parameter		Min.	Max.	Unit
Operating Temperature	Standard	-25	85	°C
	Wide	-40	85	
Storage Temperature		-40	85	°C

7.2 Power Requirement

Table 7-2 Power Requirement

Parameter	Symbol	Min.	Max.	Unit
Power Supply Voltage	V_{DD}	2.7	3.6	V

7.3 Power Consumption

Table 7-3 Power Consumption

Capacity / Mode	16 GB	32 GB	64 GB	128 GB	Unit
Operating (Max.)	80	80	80	80	mA
Standby	135	190	140	180	µA

Notes:
- All values are typical and may vary depending on flash configurations or host system settings.
- Based on USB 3.0 card reader, power consumption is measured using CrystalDiskMark 8.0.4 with sequential read/write transfers.

7.4 DC Characteristics

7.4.1 Bus Operation Conditions for 3.3V Signaling

Table 7-4 Threshold Level for High Voltage Range

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -2mA V_{DD} Min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	IOL = 2mA V_{DD} Min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time			250	ms	From 0V to V_{DD} min

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Table 7-5 Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 7-6 Threshold Level for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.58	V	

Table 7-7 Input Leakage Current for 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is disconnected.

7.4.2 Bus Signal Line Levels

Total Bus Capacitance = C_{HOST} + C_{BUS} +NC_{CARD}

Table 7-8 Bus Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection.
Capacity connected to power line	C_C		5	uF	To prevent inrush current

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7.5 AC Characteristics

7.5.1 microSD Interface Timing (Default)

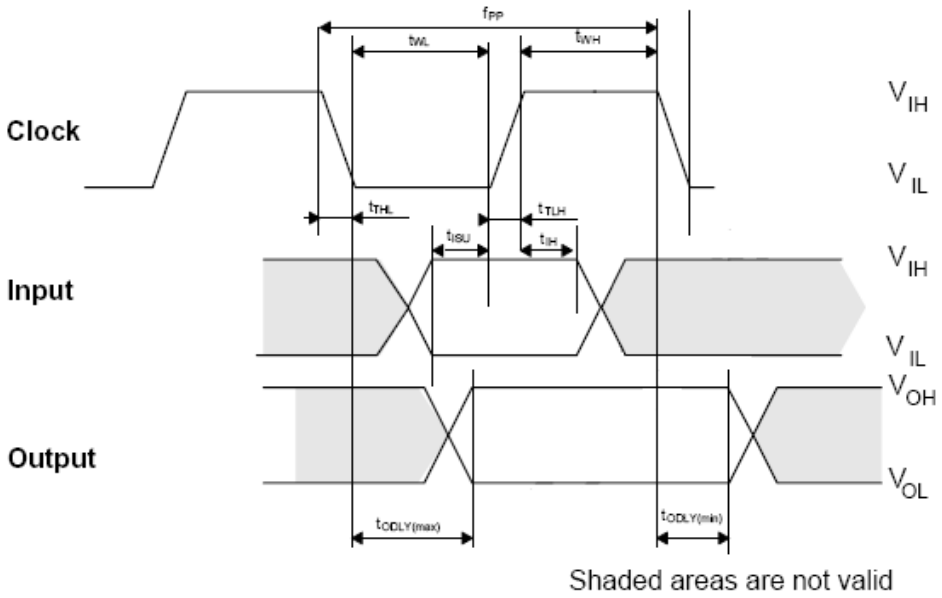


Table 7-9 microSD Interface Timing (Default)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{card} ≤ 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0[1]/100	400	kHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	10		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{card} ≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L ≤ 40 pF (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L ≤ 40 pF (1 card)

Note 1: 0Hz means to stop the clock. The given minimum frequency range is for cases where continuous clock is required.

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7.5.2 microSD Interface Timing (High-Speed Mode)

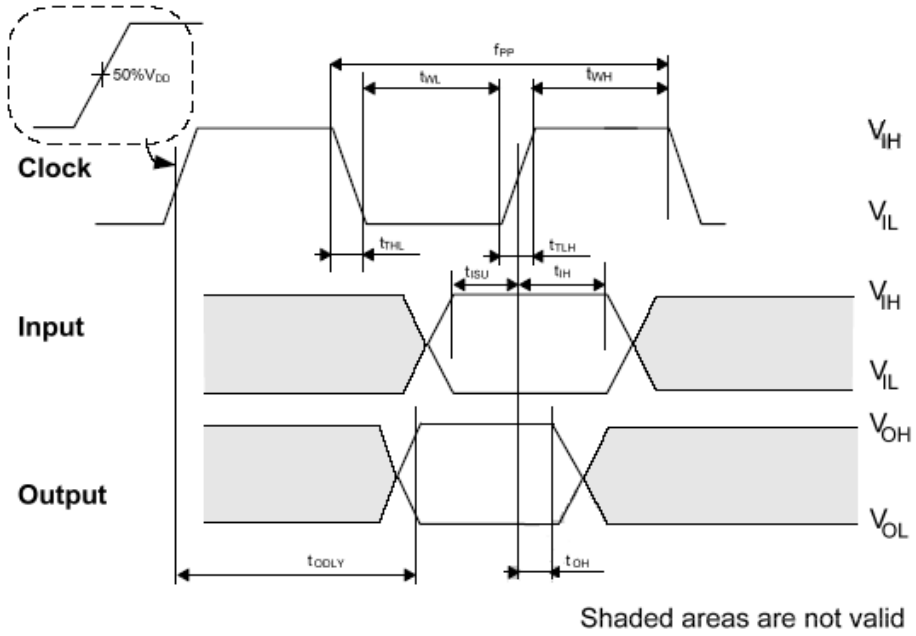


Table 7-10 microSD Interface Timing (High-Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max(V_{IL}))					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} ≤ 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{card} ≤ 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{card} ≤ 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{card} ≤ 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6		ns	C_{card} ≤ 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{card}≤ 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L ≤ 40 pF (1 card)
Output Hold Time	T_{OH}	2.5		ns	C_L ≤ 15 pF (1 card)
Total System capacitance of each line[1]	C_L		40	pF	C_L ≤ 15 pF (1 card)

Note 1: In order to satisfy severe timing, the host shall drive only one card.

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7.5.3 microSD Interface Timing (SDR12, SDR25, SDR50, and SDR104 Modes)

Input

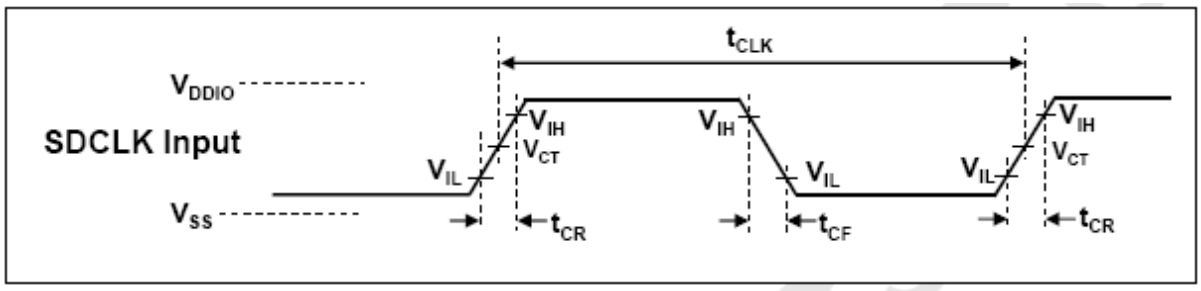


Table 7-11 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT} = 0.975V
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

Input (SDR50 and SDR104 Modes)

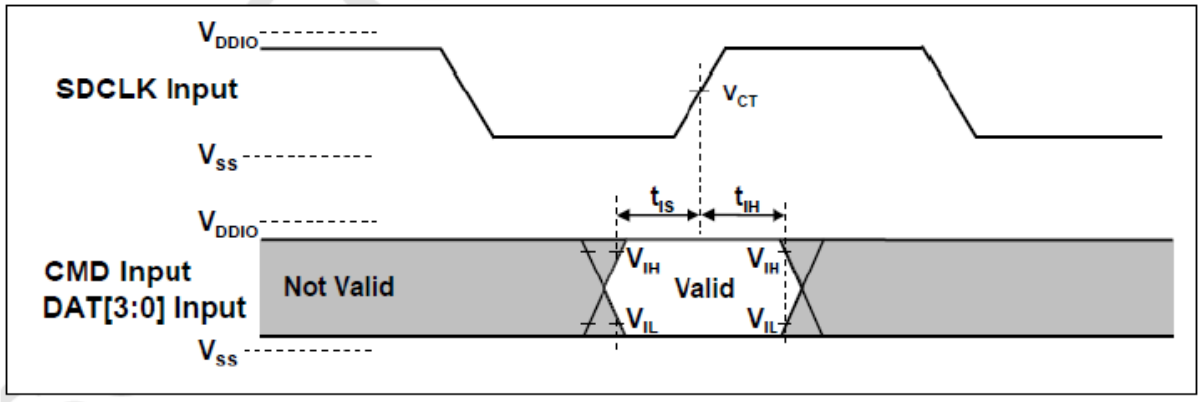


Table 7-12 Card Input Timing (SDR104 and SDR50 Modes)

Symbol	Min	Max	Unit	SDR104 Mode
t_{IS}	1.40	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V
Symbol	**Min**	**Max**	**Unit**	**SDR50 Mode**
t_{IS}	3.00	-	ns	C_{CARD} = 10pF, V_{CT} = 0.975V
t_{IH}	0.80	-	ns	C_{CARD} = 5pF, V_{CT} = 0.975V

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Output (SDR12, SDR25, and SDR50 Modes)

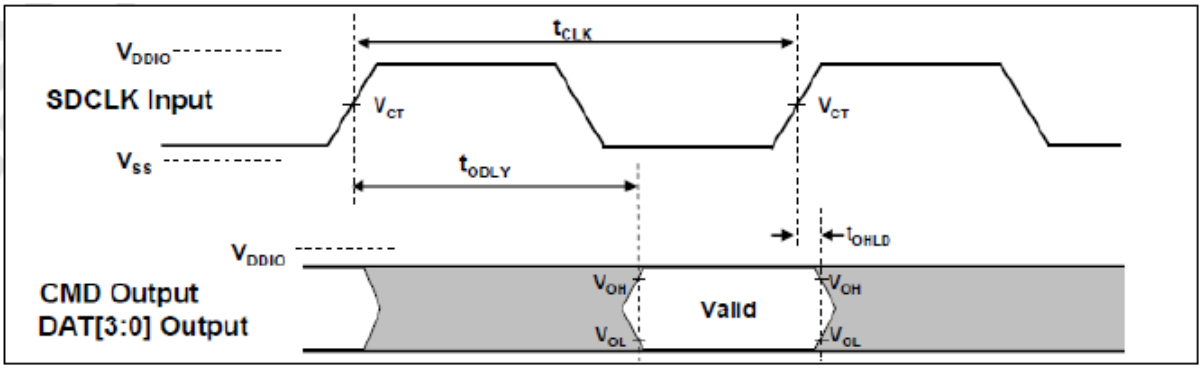


Table 7-13 Output Timing of Fixed Data Window (SDR12, SDR25, SDR50)

Symbol	Min	Max	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} ≥10.0ns, C_L=30pF, using driver Type B, for SDR50.
t_{ODLY}	-	14	ns	t_{CLK} ≥20.0ns, C_L=40pF, using driver Type B, for SDR25 and SDR12
T_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.). C_L=15pF

Output (SDR104 Mode)

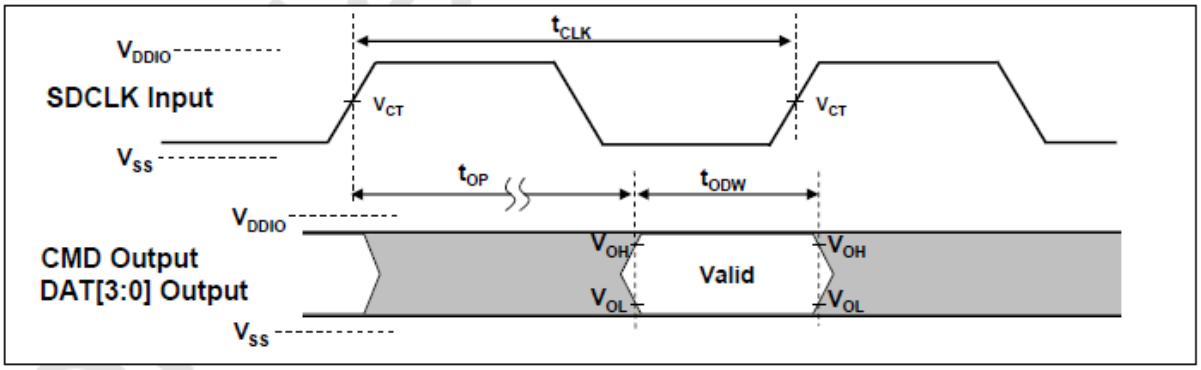


Table 7-14 Output Timing of Variable Window (SDR104)

Symbol	Min	Max	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variable due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

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7.5.4 microSD Interface Timing (DDR50 Mode)

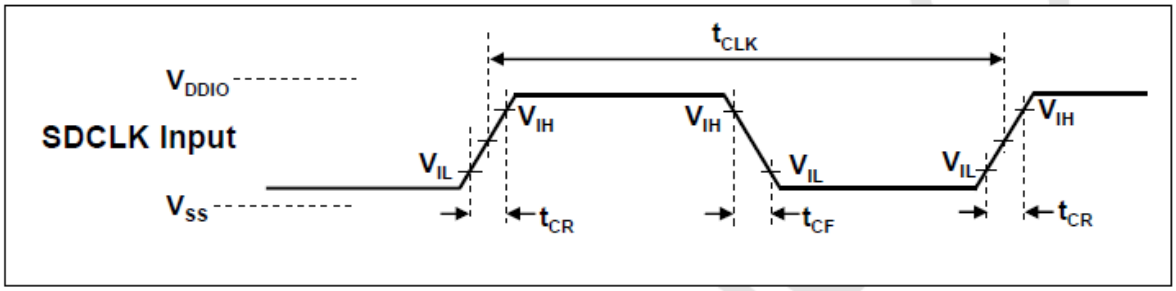
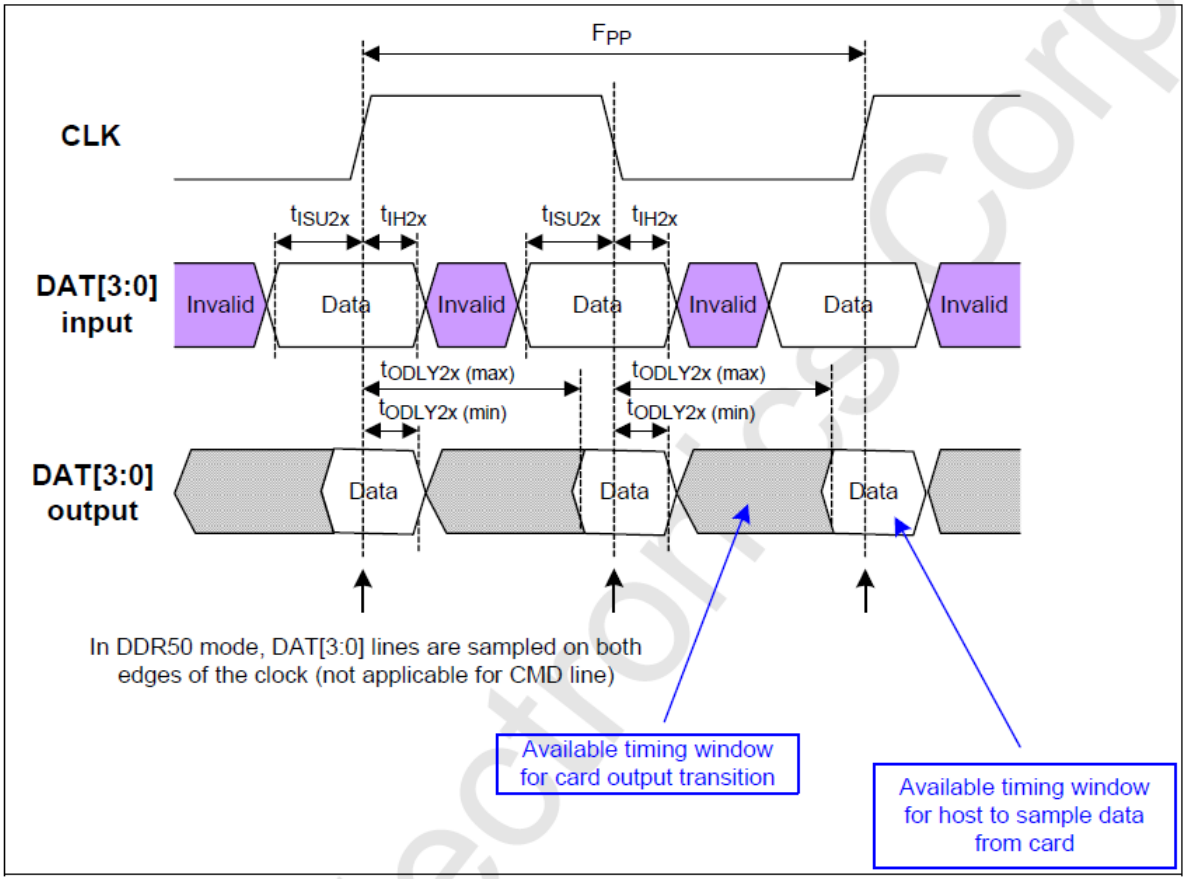


Table 7-15 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2*t_{CLK}	ns	t_{CR}, t_{CF} < 4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	



Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

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Table 7-16 Bus Timings – Parameters Values (DDR50 Mode)

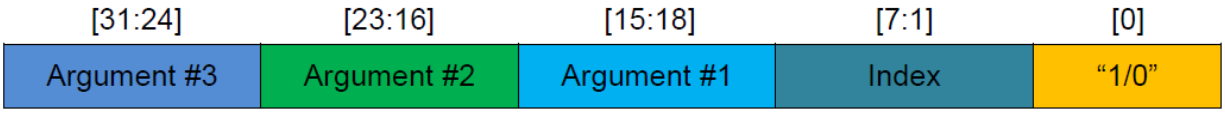
Parameter	Symbol	Min	Max	Unit	Remark
Input CMD (referenced to CLK rising edge)					
Input setup time	t_{ISU}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	$C_L \leq 30$ pF (1 card)
Output Hold time	T_{OH}	1.5	-	ns	$C_L \geq 15$ pF (1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input setup time	t_{ISU2x}	3	-	ns	$C_{card} \leq 10$ pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	$C_{card} \leq 10$ pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	$C_L \leq 25$ pF (1 card)
Output Hold time	T_{OH2x}	1.5	-	ns	$C_L \geq 15$ pF (1 card)

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8. S.M.A.R.T.

8.1 Direct Host Access to SMART Data via SD General Command (CMD56)

CMD 56 is structured as a 32-bit argument. The implementation of the general purpose functions will arrange the CMD56 argument into the following format:



- Bit [0]: Indicates Read Mode when bit is set to [1] or Write Mode when bit is cleared [0]. Depending on the function, either Read Mode or Write Mode can be used.
- Bit [7:1]: Indicates the index of the function to be executed:
  - Read Mode: Index = 0x10 Get SMART Command Information
  - Write Mode: Index = 0x08 Pre-Load SMART Command Information
- Bit [15:8]: Function argument #1 (1-byte)
- Bit [23:16]: Function argument #2 (1-byte)
- Bit [31:24]: Function argument #3 (1-byte)

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8.2 Process for Retrieving SMART Data

Step 1:

Write Mode: [0x08] Pre-Load SMART Command Information

Sequence	Command	Argument	Expected Data
Pre-Load SMART Command Information	CMD56	[0] "0" (Write Mode) [1:7] "0001 000" (Index = 0x08) [8:511] All '0' (Reserved)	No expected data

Step 2:

Read Mode – [0x10] Get SMART Command Information

Sequence	Command	Argument	Expected Data
Get SMART Command Information	CMD56	[0] "1" (Read Mode) [1:7] "0010 000" (Index = 0x10) [8:31] All '0' (Reserved)	1 sector (512 bytes) of response data byte[0-8] Flash ID byte[9-10] IC Version byte[11-12] FW Version byte[13] Reserved byte[14] CE Number byte[15] Reserved byte[16-17] Bad Block Replace Maximum byte[18] Reserved byte[32-63] Bad Block count per Die byte[64-65] Good Block Rate(%) byte[66-79] Reserved byte[80-83] Total Erase Count byte[84-95] Reserved byte[96-97] Endurance (Remain Life) (%) byte[98-99] Average Erase Count – L* byte[100-101] Minimum Erase Count – L* byte[102-103] Maximum Erase Count – L* byte[104-105] Average Erase Count – H* byte[106-107] Minimum Erase Count – H* byte[108-109] Maximum Erase Count – H* byte[110-111] Reserved byte[112-115] Power Up Count byte[116-127] Reserved byte[128-129] Abnormal Power Off Count byte[130-159] Reserved byte[160-161] Total Refresh Count byte[176-183] Product "Marker" byte[184-215] Bad Block count per Die byte[216-511] Reserved

Notes:

- *Please refer to technical note for High/Low byte definition.
- Both steps are required to retrieve SMART data: Pre-Load SMART Command followed by Get SMART Command, and must be in accordance with the SD Association standard flowchart for CMD56 (see below).

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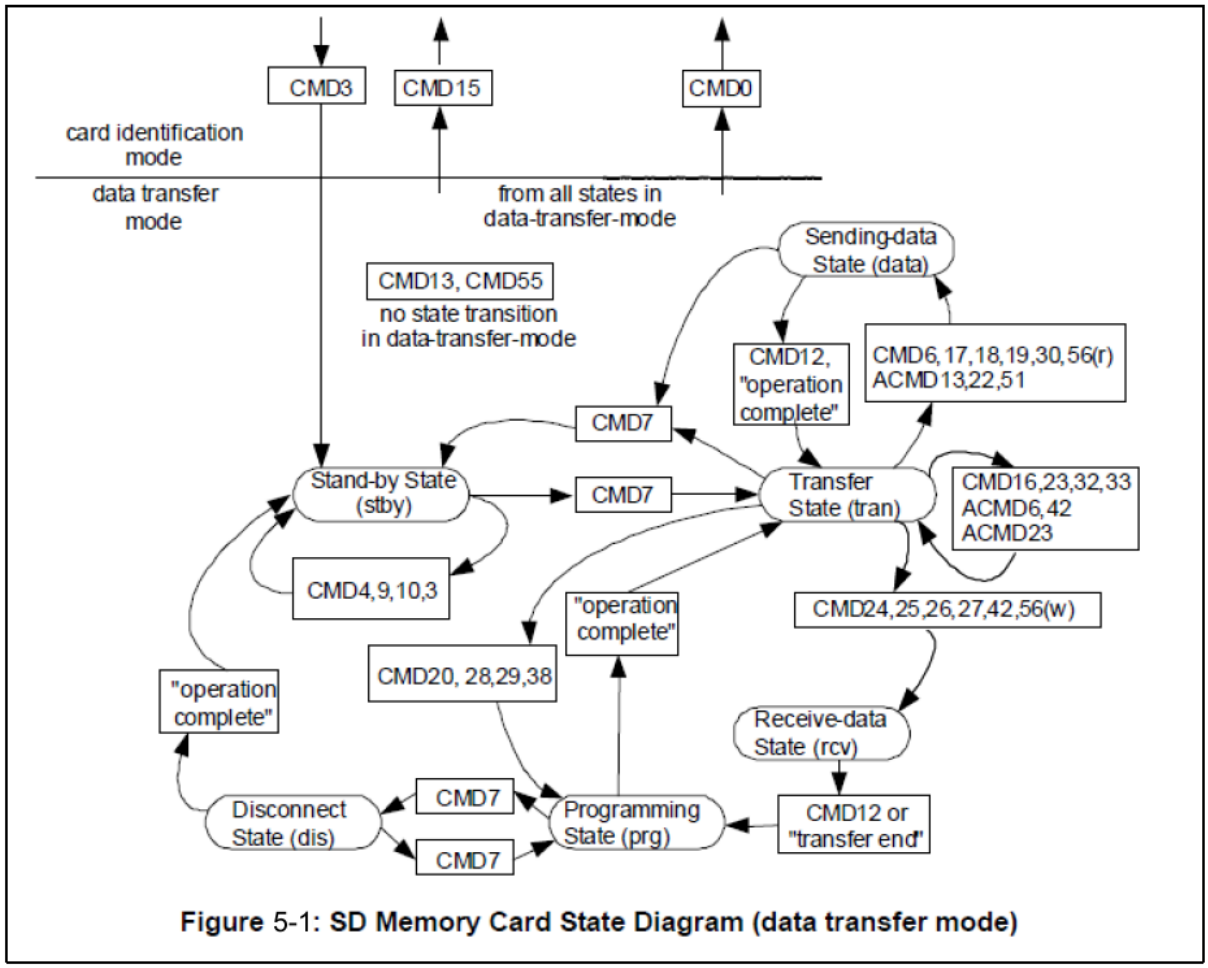
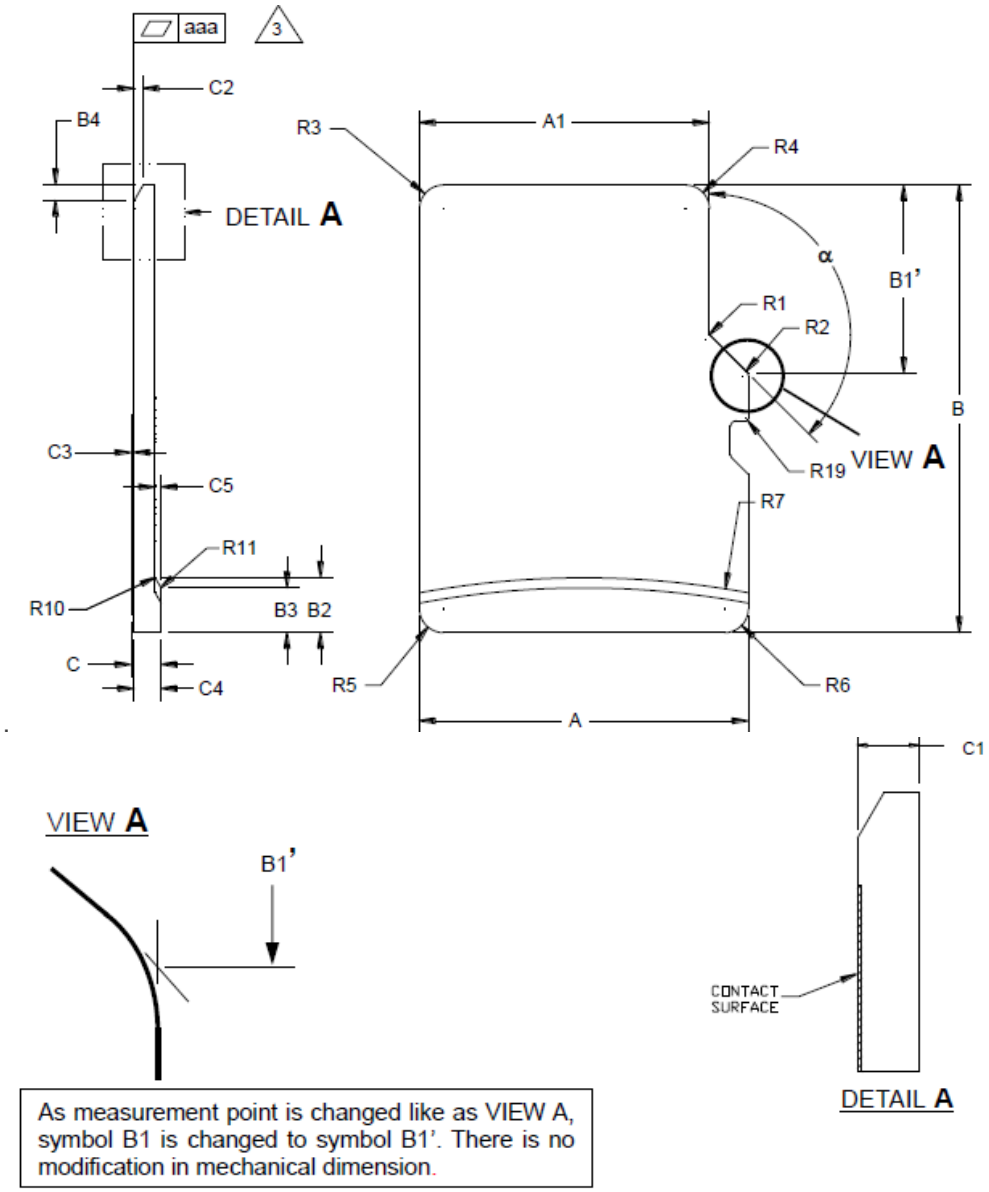


Figure 5-1: SD Memory Card State Diagram (data transfer mode)

Extracted from the SD Specifications Part 1 Physical Layer Simplified Specification Version 3.01.

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9. Mechanical Dimensions



As measurement point is changed like as VIEW A, symbol B1 is changed to symbol B1'. There is no modification in mechanical dimension.

Figure 9-1 Bottom View

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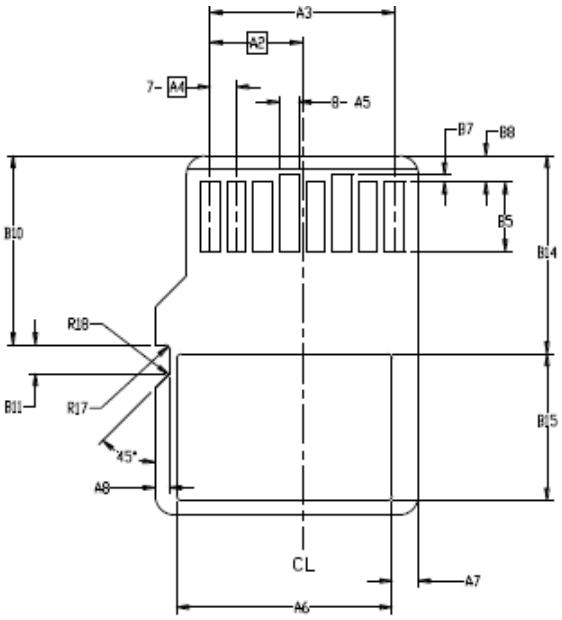


Figure 9-2 Type A Top View

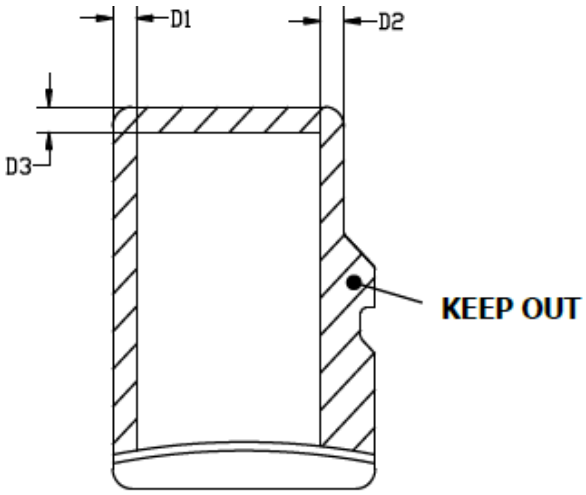


Figure 9-3 Keep-out Area

	COMMON DIMENSION			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
A10	1.35	1.40	1.45	
A11	6.50	6.60	6.70	
A12	0.50	0.55	0.60	
A13	0.40	0.45	0.50	
A14	0.05	-	-	
A15	5.71	5.81	5.91	
A16	6.47	6.57	6.67	
A17	6.62	6.72	6.82	
A18	7.38	7.48	7.58	
A19	7.75	7.85	7.95	
A20	8.55	8.65	8.75	
A21	0.90	-	-	
A22	-	-	8.50	
B	14.90	15.00	15.10	
B1'	6.13	6.23	6.33	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
B12	3.60	3.70	3.80	
B13	2.80	2.90	3.00	
B14	8.20	-	-	
B15	-	-	6.20	
B16	5.80	5.90	6.00	
B17	0.20	0.30	0.40	
B18	7.80	8.80	8.90	
B19	8.70	8.80	8.90	
B20	-	3.20	-	REF
B21	1.90	2.00	2.10	
B22	9.00	-	-	
B23	0.10	-	-	

Notes:

1. DIMENSIONING and TOLERANCING per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. COPLANARITY is additive to C1 MAX thickness.
4. All edges shall not be sharp as tested per UL1439 "Test for Sharpness of Edges on Equipment."
5. Refer to Appendix E about test method of warpage.
6. As measurement point is changed, symbol B1 is changed to symbol B1'.
7. C4 and C5 are added from Version 4.00.

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C	-	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
C4	0.80	-	1.10	
C5	0.15	-	-	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.60	0.80	0.90	
R6	0.60	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	4	-	0.15	
α	133°	135°	137°	
aaa	-	-	0.10	

Figure 9-4 microSD Package Dimensions

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10. Product Ordering Information

10.1 Product Code Designations

Apacer's CH120-MSD is available in different configurations and densities. See the chart below for a comprehensive list of options for the CH120-MSD series devices.

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	A	K	6	.	1	4	8	X	X	A	.	0	0	1	0	1

Code 1-3 (Product Line & Form Factor)	CH120-MSD
Code 5-6 (Model/Solution)	CH120
Code 7-8 (Product Capacity)	8G: 16GB 8H: 32GB 8J: 64GB 8K: 128GB
Code 9 (Flash Type & Product Temp)	S: 3D SLC lite-X Standard Temperature T: 3D SLC lite-X Wide Temperature
Code 10 (Product Spec)	microSD Card
Code 12-14 (Version Number)	Random numbers generated by system
Code 15-16 (Firmware Version)	

10.2 Valid Combinations

The following table lists the available models of the CH120-MSD series which are in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Capacity	Standard Temperature	Wide Temperature
16GB	AK6.148GSA.00101	AK6.148GTA.00101
32GB	AK6.148HSA.00101	AK6.148HTA.00101
64GB	AK6.148JSA.00101	AK6.148JTA.00101
128GB	AK6.148KSA.00101	AK6.148KTA.00101

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Revision History

Revision	Description	Date
1.0	Initial release	2/6/2024
1.1	Added 128GB support	10/14/2024
1.2	Updated document format and template	1/14/2025

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